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Homework 2

**Chapter 3**

1. The categories are processor-memory, processor-I/O, data processing, and control
2. **Instruction Address Calculation**: Determine the address of the next instruction to be executed.

**Instruction Fetch:** Read instruction from its memory location into the processor.

Instruction Operation Decoding: Analyze instruction to determine type of operation to be performed and operands to be used.

**Operand Address Calculation:** If the operation involves reference to an operand in memory or available via I/O then decides the address of the operand.

**Operand Fetch:** Fetch the operand from memory or read it in from I/O.

**Data Operation**: Perform the operation indicated in the instruction.

**Operand Store:** Write the result into memory or out to I/O.

1. **Disabling Interrupts:** Processor has the ability to and will ignore the specific interrupts. Those interrupts remain pending and will be checked after the processor has enabled interrupts.

**Interrupt Service Routine:** Priorities assigned to the different types of interrupts. Interrupts service routines with higher priorities can interrupt ones with lower priority in which case the ISR with the lower priority is put on the stack until that ISR is completed

1. 1. 2^(32-8) = 2^24 = 16,777,216 bytes = 16MB, (8 bits=1byte for the opcode)
   2. 1. Instruction and data transfers would take three bus cycles each, one for the address and two for the data. Because the bus is 32 bits the whole address can be transferred to memory at once and decoded there but since the data bus is only 16 it requires 2 bus cycles to fetch 32-bit instruction and operand.
      2. Instruction and data transfers would take four bus cycles each, two for the address and two for the data. That till have the processor perform two transmissions in order to send to memory the whole 32-bit address. This will require more complex memory interface control to latch the two halves of the address before it performs access to it. Since the data bus is 16 bits the processor will need 2 bus cycles to fetch the 32-bit instruction or operand.
   3. Program Counter needs 24 bits and Instruction Register needs 32-bits.

**Chapter 4**

1. As access time becomes faster, the cost per bit increases. As memory size increases, the cost per bit is smaller. With greater capacity, the access time becomes slower.
2. With the names I, J, and M we have I as the cache line number, J as the main memory block number, and M as the number of lines in the cache.
3. The two fields are Tag and Word. The Tag field uniquely identifies a block of main memory. The Word is what is to be placed in the block of memory.
4. The fields are Tag, Set, and Word. Tag identifies a block of main memory, set specifies one of the 2^s blocks of main memory and Word is what is to be placed in the main memory.
5. Special locality refers to the tendency of execution to involve a number of memory locations that are clustered. Temporal locality deals with the tendency for a processor to access memory locations that have been used recently.